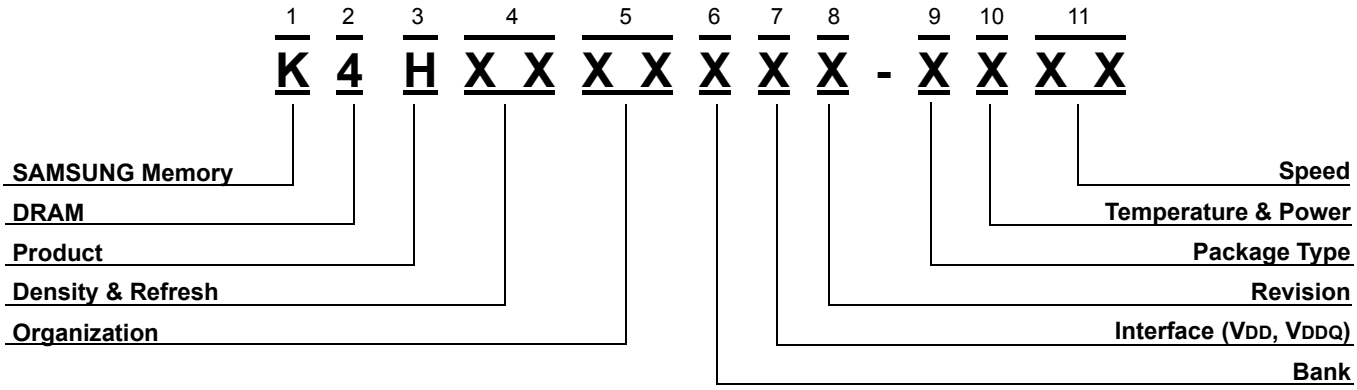
DDR SDRAM Product Guide

July 2006

Memory Division

A. DDR SDRAM Component Ordering Information



1. SAMSUNG Memory : K

2. DRAM : 4

3. Product

H : DDR SDRAM

4. Density & Refresh

28 : 128Mb, 4K/64ms
56 : 256Mb, 8K/64ms
51 : 512Mb, 8K/64ms
1G: 1Gb, 8K/64ms
2G: 2Gb, 8K/64ms

5. Organization

04 : x 4
06 : x 4 Stack
07 : x 8 Stack
08 : x 8
16 : x16

6. Bank

3 : 4 Banks

7. Interface (VDD, VDDQ)

8 : SSTL-2 (2.5V, 2.5V)

8. Revision

M : 1st Gen.
A : 2nd Gen.
B : 3rd Gen.
C : 4th Gen.
D : 5th Gen.
E : 6th Gen.
F : 7th Gen.
G : 8th Gen.
H : 9th Gen.

9. Package Type

T : TSOP II
N : sTSOP II
G : FBGA
U : TSOP II (Lead Free)*1
V : sTSOP II (Lead Free)*1
Z : FBGA (Lead Free)*1

(note 1: All of Pb-free product are in compliance with RoHS)

10. Temperature & Power

C : Commercial Temp.(0°C ~ 70°C) & Normal Power
L : Commercial Temp.(0°C ~ 70°C) & Low Power
I : Industrial Temp.(-40°C ~ 85°C) & Normal Power
P : Industrial Temp.(-40°C ~ 85°C) & Low Power

11. Speed

CC : DDR400 (200MHz @ CL=3, tRCD=3, tRP=3)
B3 : DDR333 (166MHz @ CL=2.5, tRCD=3, tRP=3)
A2 : DDR266 (133MHz @ CL=2 , tRCD=3, tRP=3)
B0 : DDR266 (133MHz @ CL=2.5, tRCD=3, tRP=3)

B. DDR SDRAM Component Product Guide

Density	Bank	Part Number	Package & Power, Temp.*2(-C/-L/-I/-P) & Speed *3	Org.	Inter-face	Ref.	Power (V)	PKG*1	Avail.
256Mb E-die	4Banks	K4H560438E	T(U)CB3/CA2/CB0 T(U)LB3/LA2/LB0	64M x 4	SSTL_2	8K/64m	2.5 ± 0.2V*4	66pinTSOP(II)	Now
			G(Z)CCC/CB3 G(Z)LCC/LB3					60ball FBGA	
		K4H560838E	T(U)CCC/CB3/CA2/CB0 T(U)LCC/LB3/LA2/LB0	32M x 8				66pin TSOP(II)	
			G(Z)CCC/CB3 G(Z)LCC/LB3					60ball FBGA	
256Mb H-die		K4H560438H	UCA2/CB0 ULA2/LB0	64M x 4				66pin TSOP(II)	
			ZCCC/CB3 ZLCC/LB3					60ball FBGA	
		K4H560838H	UCCC/CB3/CA2/CB0 ULCC/LB3/LA2/LB0	32M x 8				66pin TSOP(II)	
			ZCCC/CB3 ZLCC/LB3					60ball FBGA	
		K4H561638H	UCCC/CB3/CA2/CB0 ULCC/LB3/LA2/LB0	16M x 16				66pin TSOP(II)	
			ZCCC/CB3 ZLCC/LB3					60ball FBGA	
		K4H561638H	UIB3/IA2/IB0 UPB3/PA2/PB0	16M x 16				66pin TSOP(II)	
			ZIB3/IA2/IB0 ZPB3/PA2/PB0					60ball FBGA	
stacked 512Mb E-die		K4H510638E	T(U)CA2/CB0 T(U)LA2/LB0	128M x 4				66pin stacked TSOP(II)	
		K4H510738E		64M x 8					
stacked 512Mb H-die		K4H510638H	UCA2/CB0 ULA2/LB0	128M x 4					
		K4H510738H		64M x 8					
512Mb C-die*5		K4H510438C	UCB3/CA2/CB0 ULB3/LA2/LB0	128M x 4				66pin TSOP(II)	
			ZCCC/CB3 ZLCC/LB3					60ball FBGA	
		K4H510838C	UCCC/CB3/CA2/CB0 ULCC/LB3/LA2/LB0	64M x 8				66pin TSOP(II)	
			ZCCC/CB3 ZLCC/LB3					60ball FBGA	
		K4H511638C	UCCC/CB3/CA2/CB0 ULCC/LB3/LA2/LB0	32M x 16				66pin TSOP(II)	
			ZCCC/CB3 ZLCC/LB3					60ball FBGA	
		K4H510838C	UIB3/IA2/IB0 UPB3/PA2/PB0	64M x 8				66pin TSOP(II)	
			ZIB3/IA2/IB0 ZPB3/PA2/PB0					60ball FBGA	
		K4H511638C	UIB3/IA2/IB0 UPB3/PA2/PB0	32M x 16				66pin TSOP(II)	
			ZIB3/IA2/IB0 ZPB3/PA2/PB0					60ball FBGA	
512Mb D-die*5		K4H510838D	UCCC/CB3/CA2/CB0 ULCC/LB3/LA2/LB0	64M x 8				66pin TSOP(II)	
			VCCC/CB3/CA2/CB0 VLCC/LB3/LA2/LB0					54pin sTSOP(II)	
		K4H511638D	UCCC/CB3/CA2/CB0 ULCC/LB3/LA2/LB0	32M x 16				66pin TSOP(II)	
stacked 1Gb C-die*5		K4H1G0638C	UCA2/CB0 ULA2/LB0	256M x 4				66pin TSOP(II)	
		K4H1G0738C		128M x 8					
1Gb A-die		K4H1G0438A	UCCC/CB3/CA2/CB0 ULCC/LB3/LA2/LB0	256M x 4				66pin TSOP(II)	
		K4H1G0838A		128M x 8					
stacked 2Gb A-die*5		K4H2G0638A	UCCC/CB3/CA2/CB0, ULCC/LB3/LA2/LB0	512M x 4				66pin TSOP(II)	

Note 1:
T : TSOP II U:TSOP II (Lead Free)
N : sTSOP II V:sTSOP II (Lead Free)
G: FBGA Z:FBGA II (Lead Free)

Note 2:

C	Commercial Temperature, Normal Power
L	Commercial Temperature, Low Power
I	Industrial Temperature, Normal Power
P	Industrial Temperature, Low Power

Note 3:

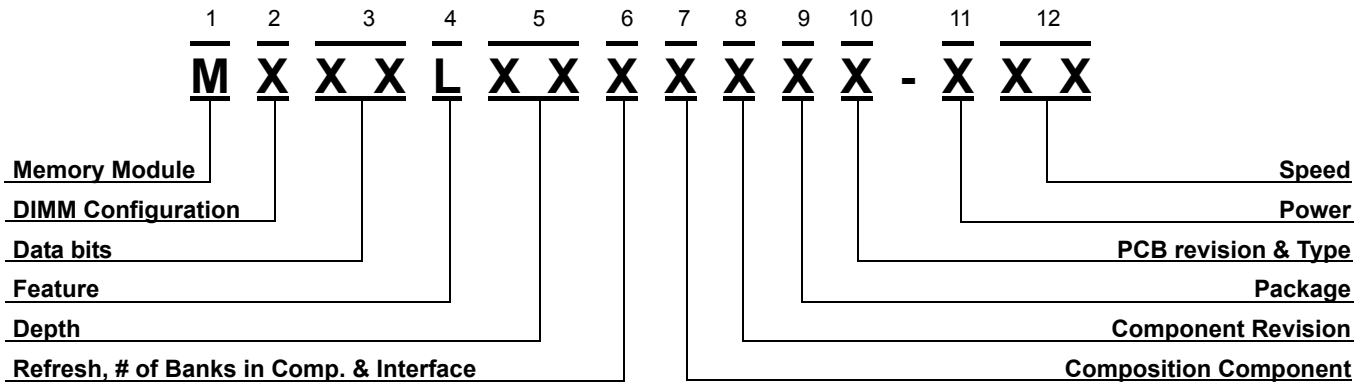
	133Mhz	166Mhz	200Mhz
CL = 2	DDR266(A2)	-	-
CL = 2.5	DDR266(B0)	DDR333(B3)	-
CL = 3	-	-	DDR400(CC)

Note 4:

	DDR400	DDR333/266
VDD/VDDQ	2.6V ± 0.1V	2.5V ± 0.2V

Note 5: All of DDR components support both Leaded and lead-free. And from 512Mb C-die, D-die and 1Gb A-die Lead-free is default PKG Type.

C. DDR SDRAM Module Ordering Information



1. Memory Module : M

2. DIMM Configuration

3 : DIMM
4 : SODIMM

3. Data Bits

68 : x64 184pin Unbuffered DIMM
81 : x72 184pin ECC unbuffered DIMM
83 : x72 184pin Registered DIMM
12 : x72 184pin Low Profile Registered DIMM
70 : x64 200pin Unbuffered SODIMM
63 : x64 172pin Micro DIMM

4. Feature

L : DDR SDRAM (2.5V VDD)

5. Depth

16 : 16M
32 : 32M
64 : 64M
28 : 128M
56 : 256M
51 : 512M
17 : 16M (for 128Mb/512Mb)
33 : 32M (for 128Mb/512Mb)
65 : 64M (for 128Mb/512Mb)
29 : 128M (for 128Mb/512Mb)
57 : 256M (for 512Mb)

6. Refresh, # of Banks in comp. & Interface

1 : 4K/ 64ms Ref., 4Banks & SSTL-2
2 : 8K/ 64ms Ref., 4Banks & SSTL-2

7. Composition Component

0 : x 4
3 : x 8
4 : x16
8 : x 4 Stack
9 : x 8 Stack

8. Component Revision

M : 1st Gen.
A : 2nd Gen.
B : 3rd Gen.
C : 4th Gen.
D : 5th Gen.
E : 6th Gen.
F : 7th Gen.
G : 8th Gen
H : 9th Gen.

9. Package

T : TSOP II (400mil)
U : TSOP II*1 (Lead Free)
N : sTSOP
V : sTSOP II*1 (Lead Free)
G : FBGA
Z : FBGA*1 (Lead Free)

(note 1 : All of Pb-free product are in compliance with RoHS)

10. PCB Revision & Type

0 : Mother PCB
1 : 1st Rev.
2 : 2nd Rev.
3 : 3rd Rev.
S : Reduced layer PCB

11. Temp & Power

C : Commercial Temp.(0°C ~ 70°C) & Normal Power
L : Commercial Temp.(0°C ~ 70°C) & Low Power

12. Speed

CC : DDR400 (200MHz @ CL=3, tRCD=3, tRP=3)
B3 : DDR333 (166MHz @ CL=2.5, tRCD=3, tRP=3)
A2 : DDR266 (133MHz @ CL=2 , tRCD=3, tRP=3)
B0 : DDR266 (133MHz @ CL=2.5, tRCD=3, tRP=3)

D. DDR SDRAM Module Product Guide

Org.	Den-sity	Part Number	Speed	Composition	Comp. Version	Voltage	Internal Banks	External Banks	PKG*1	Feature	Avail.
184Pin DDR Unbuffered DIMM											
32Mx 64	256MB	M368L3223ET(U)N	CB3, LB3	32Mx 8 * 8pcs	256Mb 6th	2.5 ± 0.2V*3	4	1	66TSOP(II)	SS,1250mil	Now
		M368L3223ET(U)M	CCC, LCC	32Mx 8 * 8pcs							
		M368L3223HUS	CCC/CB3, LCC/LB3	32Mx 8 * 8pcs	256Mb 9th						
		M368L3324CUS*2	CCC/CB3, LCC/LB3	32Mx 16 * 4pcs	512Mb 4th						
		M368L3324DUS*2	CCC/CB3, LCC/LB3	32Mx 16 * 4pcs	512Mb 5th						
32Mx 72		M381L3223ET(U)M	CCC/CB3, LCC/LB3	32Mx 8 * 9pcs	256Mb 6th						
		M381L3223HUM	CCC/CB3, LCC/LB3	32Mx 8 * 9pcs	256Mb 9th						
64Mx 64	512MB	M368L6423ET(U)N	CB3, LB3	32Mx 8 * 16pcs	256Mb 6th			2		DS,1250mil	
		M368L6423ET(U)M	CCC, LCC	32Mx 8 * 16pcs	256Mb 6th						
		M368L6423HUN	CCC/CB3, LCC/LB3	64Mx 8 * 8pcs	256Mb 9th			1		SS,1250mil	
		M368L6523CUS*2	CCC/CB3, LCC/LB3	64Mx 8 * 8pcs	512Mb 4th						
		M368L6523DUS*2	CCC/CB3, LCC/LB3	64Mx 8 * 8pcs	512Mb 5th						
64Mx 72		M381L6423ET(U)M	CCC/CB3, LCC/LB3	32Mx 8 * 18pcs	256Mb 6th			2		DS,1250mil	
		M381L6423HUM	CCC/CB3, LCC/LB3	32Mx 8 * 18pcs	512Mb 3rd						
		M381L6523CUM*2	CCC/CB3, LCC/LB3	64Mx 8 * 9pcs	512Mb 4th			1		SS,1250mil	
		M381L6523DUM*2	CCC/CB3, LCC/LB3	64Mx 8 * 9pcs	512Mb 5th						
128Mx 64	1GB	M368L2923CUN*2	CCC/CB3, LCC/LB3	64Mx 8 * 16pcs	512Mb 4th			2		DS,1250mil	
		M368L2923DUN*2	CCC/CB3, LCC/LB3		512Mb 5th						
128Mx 72		M381L2923CUM*2	CCC/CB3, LCC/LB3	64Mx 8 * 18pcs	512Mb 4th						
		M381L2923DUM*2	CCC/CB3, LCC/LB3		512Mb 5th						

Note 1:(All of DDR DIMMs can support Pb-free)
T : TSOP II U : TSOP II (Lead Free)
N : sTSOP II V : sTSOP II (Lead Free)
G : FBGA Z : FBGA (Lead Free)

Note 2: All of DDR components support both Leaded and lead-free. And from 512Mb C-die, D-die and 1Gb A-die Lead-free is default PKG Type.

Note 3:

	DDR400	DDR333/266
VDD/VDDQ	2.6V ± 0.1V	2.5V ± 0.2V

184Pin DDR Low Profile Registered DIMM

Org.	Den-sity	Part Number	Speed	Composition	Comp. Version	Voltage	Internal Banks	External Banks	PKG*1	Feature	Avail.
32Mx 72	256MB	M312L3223ET(U)S	CA2/CB0, LA2/LB0	32Mx 8 * 9pcs	256Mb 6th	2.5 ± 0.2V*3	4	1	66pin TSOP(II)	DS,1200mil	Now
		M312L3223HUS	CA2/CB0, LA2/LB0	32Mx 8 * 9pcs	256Mb 9th						
		M312L3223EG(Z)0	CCC/CB3, LCC/LB3	32Mx 8 * 9pcs	256Mb 6th				60ball FBGA	DS,1125mil	
		M312L3223HZ0	CCC/CB3, LCC/LB3	32Mx 8 * 9pcs	256Mb 9th						
64Mx 72	512MB	M312L6423ET(U)S	CA2/CB0, LA2/LB0	32Mx 8 * 18pcs	256Mb 6th			2	66pin TSOP(II)	DS,1200mil	
		M312L6423HUS	CA2/CB0, LA2/LB0	32Mx 8 * 18pcs	256Mb 9th						
		M312L6420ET(U)S	CA2/CB0, LA2/LB0	64Mx 4 * 18pcs	256Mb 6th			1			
		M312L6420HUS	CA2/CB0, LA2/LB0	64Mx 4 * 18pcs	256Mb 9th						
		M312L6523CUS*2	CA2/CB0, LA2/LB0	64Mx 8 * 9pcs	512Mb 4th						
		M312L6420EG(Z)0	CCC/CB3, LCC/LB3	64Mx 4 * 18pcs	256Mb 6th			1	60ball FBGA	DS,1125mil	
		M312L6420HZ0	CCC/CB3, LCC/LB3	64Mx 4 * 18pcs	256Mb 9th						
		M312L6423EG(Z)0	CCC/CB3, LCC/LB3	32Mx 8 * 18pcs	256Mb 6th			2			
		M312L6423HZ0	CCC/CB3, LCC/LB3	32Mx 8 * 18pcs	256Mb 9th						
		M312L6523CZ0*2	CCC/CB3, LCC/LB3	64Mx 8 * 9pcs	512Mb 4th			1		SS,1125mil	
128Mx 72	1GB	M312L2828ET(U)0	CA2/CB0, LA2/LB0	st.128Mx 4 * 18pcs	256Mb 6th			2	66pin TSOP(II)	DS,1200mill	
		M312L2828HU0	CA2/CB0, LA2/LB0	st.128Mx 4 * 18pcs	256Mb 9th						
		M312L2923CUS*2	CA2/CB0, LA2/LB0	64Mx 8 * 18pcs	512Mb 4th						
		M312L2920CUS*2	CA2/CB0, LA2/LB0	128Mx 4 * 18pcs	512Mb 4th			1			
		M312L2820EG(Z)0	CCC/CB3, LCC/LB3	64Mx 4 * 36pcs	256Mb 6th			2	60ball FBGA	DS,1200mil	
		M312L2820HZ0	CCC/CB3, LCC/LB3	64Mx 4 * 36pcs	256Mb 9th			2			
		M312L2920CZ0*2	CCC/CB3, LCC/LB3	128Mx 4 * 18pcs	512Mb 4th			1		DS,1125mil	
		M312L2923CZ0*2	CCC/CB3, LCC/LB3	128Mx 8 * 18pcs	512Mb 4th			2			
256Mx 72	2GB	M312L5628CU0*2	CA2/CB0, LA2/LB0	st.256Mx 4 * 18pcs	512Mb 4th			2	66pin TSOP(II)	DS,1200mil	
		M312L5720CZ0*2	CCC/CB3, LCC/LB3	128Mx 4 * 36pcs	512Mb 4th				60ball FBGA		
		M312L5620AUS*2	CCC/CB3/CA2/CB0 LCC/LB3/LA2/LB0	256Mx 4 * 18pcs	1Gb 2nd			1	66pin TSOP(II)		
		M312L5623AUS*2	CCC/CB3/CA2/CB0 LCC/LB3/LA2/LB0	128Mx 8 * 18pcs	1Gb 2nd			2			
512Mx72	4GB	M312L5128AU0*2	CB3/CA2/CB0 LB3/LA2/LB0	st.512MX 4 * 18pcs	1Gb 2nd					DS,1200mil	
		M312L5128AU1*2	CCC LCC	st.512MX 4 * 18pcs	1Gb 2nd						

Note 1:(All of DDR DIMMs can support Pb-free)
T : TSOP II U : TSOP II (Lead Free)
N : sTSOP II V : sTSOP II (Lead Free)
G : FBGA Z : FBGA (Lead Free)

Note 2: All of DDR components support both Leaded and lead-free. And from 512Mb C-die, D-die and 1Gb A-die Lead-free is default PKG Type.

Note 3:

	DDR400	DDR333/266
VDD/VDDQ	2.6V ± 0.1V	2.5V ± 0.2V

200Pin DDR SODIMM											
Org.	Den-sity	Part Number	Speed	Composition	Comp. Version	Voltage	Internal Banks	External Banks	PKG*1	Feature	Avail.
16Mx64	128MB	M470L1624HU0	CCC/CB3/CA2/CB0 LCC/LB3/LA2/LB0	16Mx 16 * 4pcs	256Mb 9th	2.5 ± 0.2V*3	4	1	66pin TSOP(II)	SS,1250mi	Now
32Mx 64	256MB	M470L3224HU0	CCC/CB3/CA2/CB0 LCC/LB3/LA2/LB0	16Mx 16 * 8pcs	256Mb 9th			2		DS,1250mi	
		M470L3324CU0*2	CCC/CB3/CA2/CB0 LCC/LB3/LA2/LB0	32Mx 16 * 4pcs	512Mb 4th			1		SS,1250mi	
		M470L3324DU0*2	CCC/CB3/CA2/CB0 LCC/LB3/LA2/LB0	32Mx 16 * 4pcs	512Mb 5th						
64Mx 64	512MB	M470L6524CU0*2	CCC/CB3/CA2/CB0 LCC/LB3/LA2/LB0	32Mx 16 * 8pcs	512Mb 4th			2		DS,1250mi	
		M470L6524DU0*2	CCC/CB3/CA2/CB0 LCC/LB3/LA2/LB0	32Mx 16 * 8pcs	512Mb 5th						
128Mx 64	1GB	M470L2923DV0*2	CCC/CB3/CA2/CB0 LCC/LB3/LA2/LB0	64Mx 8 * 16pcs	512Mb 5rd				54pin sTSOP(II)		

Note 1:(All of DDR DIMMs can support Pb-free)
T : TSOP II U : TSOP II (Lead Free)
N : sTSOP II V : sTSOP II (Lead Free)
G : FBGA Z : FBGA (Lead Free)

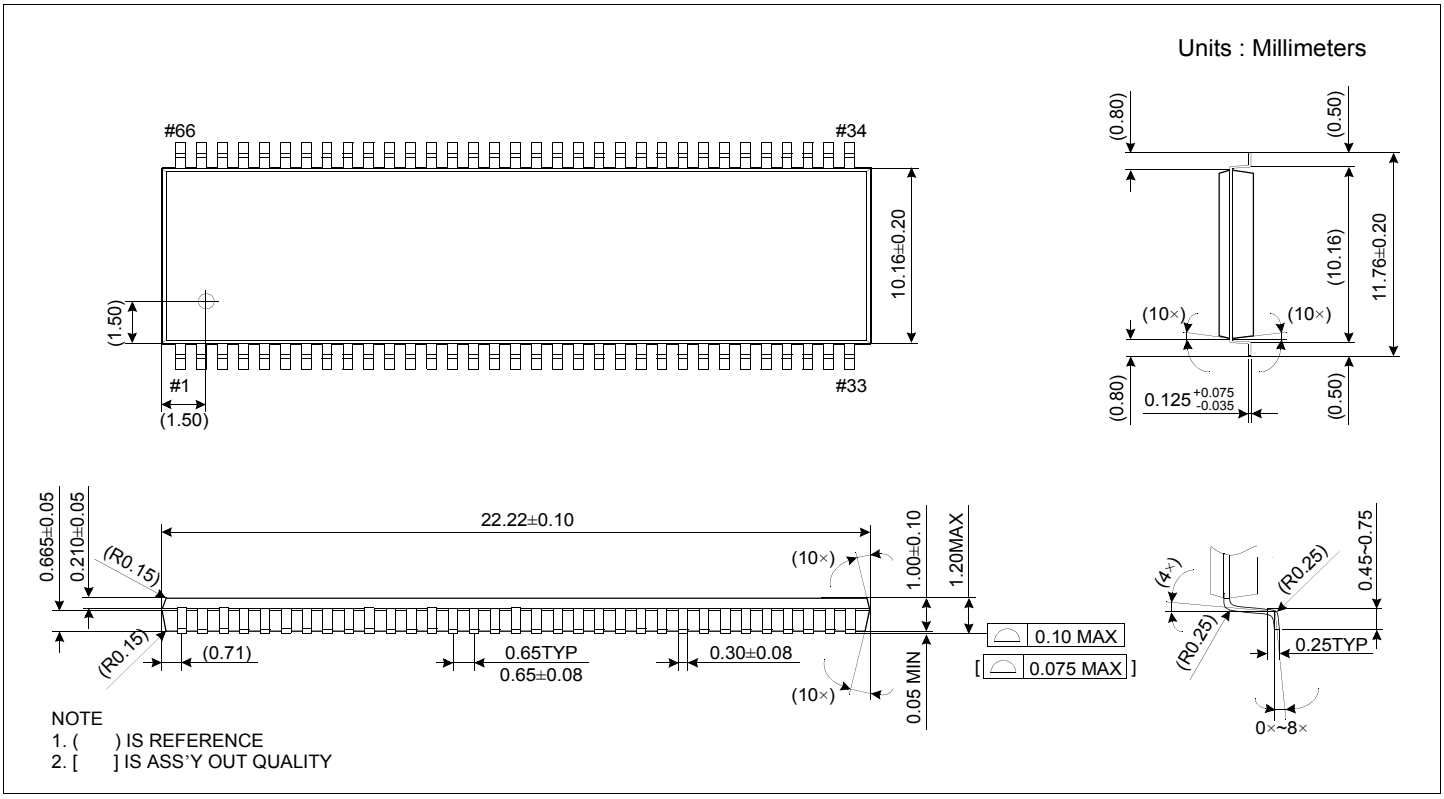
Note 2: All of DDR components support both Leaded and lead-free. And from 512Mb C-die, D-die and 1Gb A-die Lead-free is default PKG Type.

Note 3:

	DDR400	DDR333/266
VDD/VDDQ	2.6V ± 0.1V	2.5V ± 0.2V

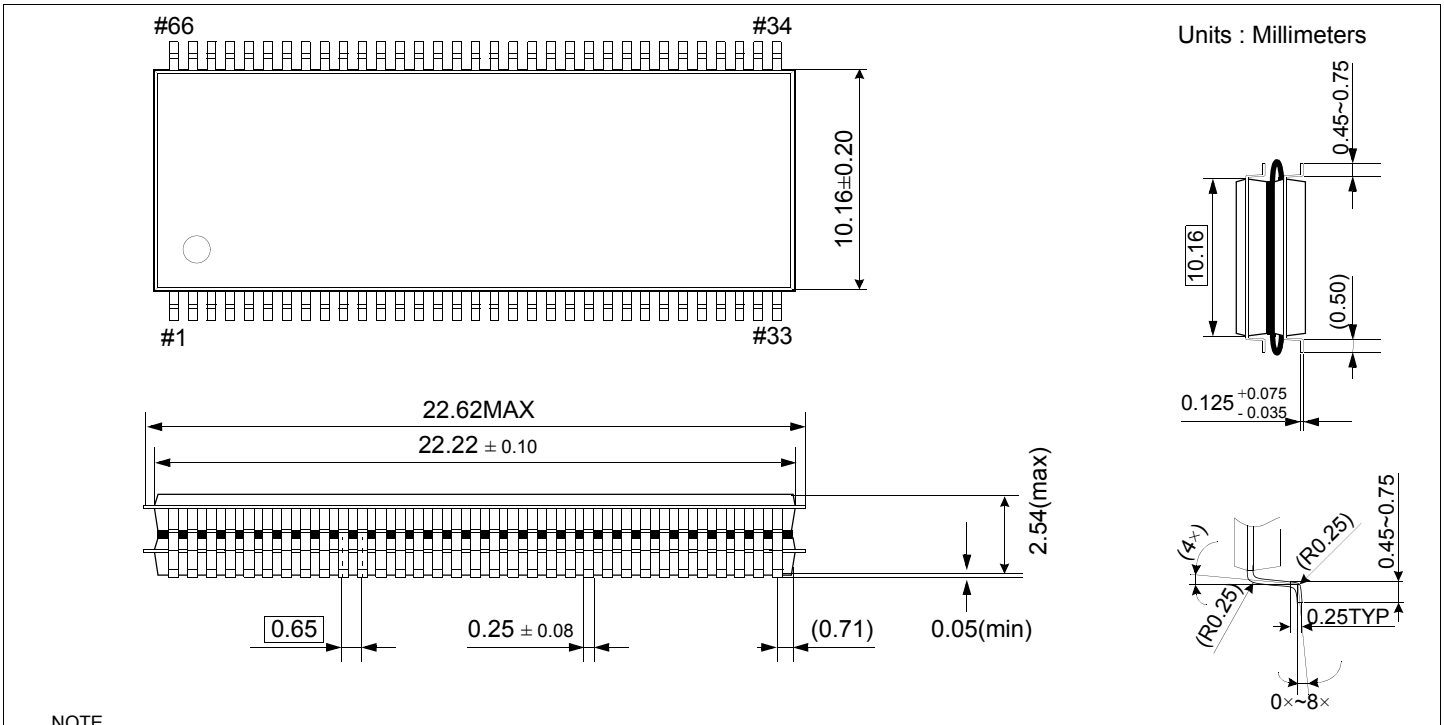
E. Package Dimension

66pin TSOP-II



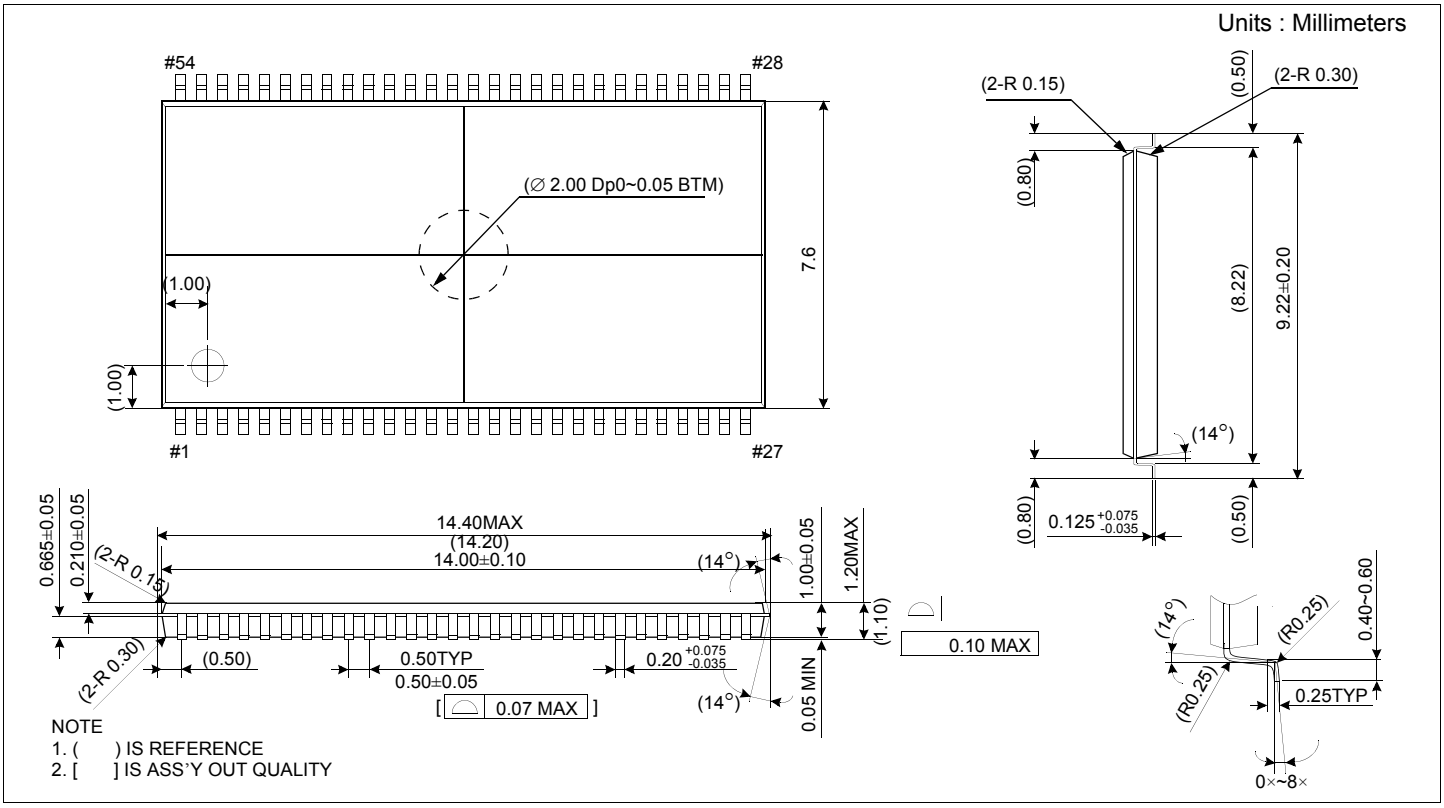
NOTE
1. ( ) IS REFERENCE
2. [ ] IS ASS'Y OUT QUALITY

66pin TSOP-II stack

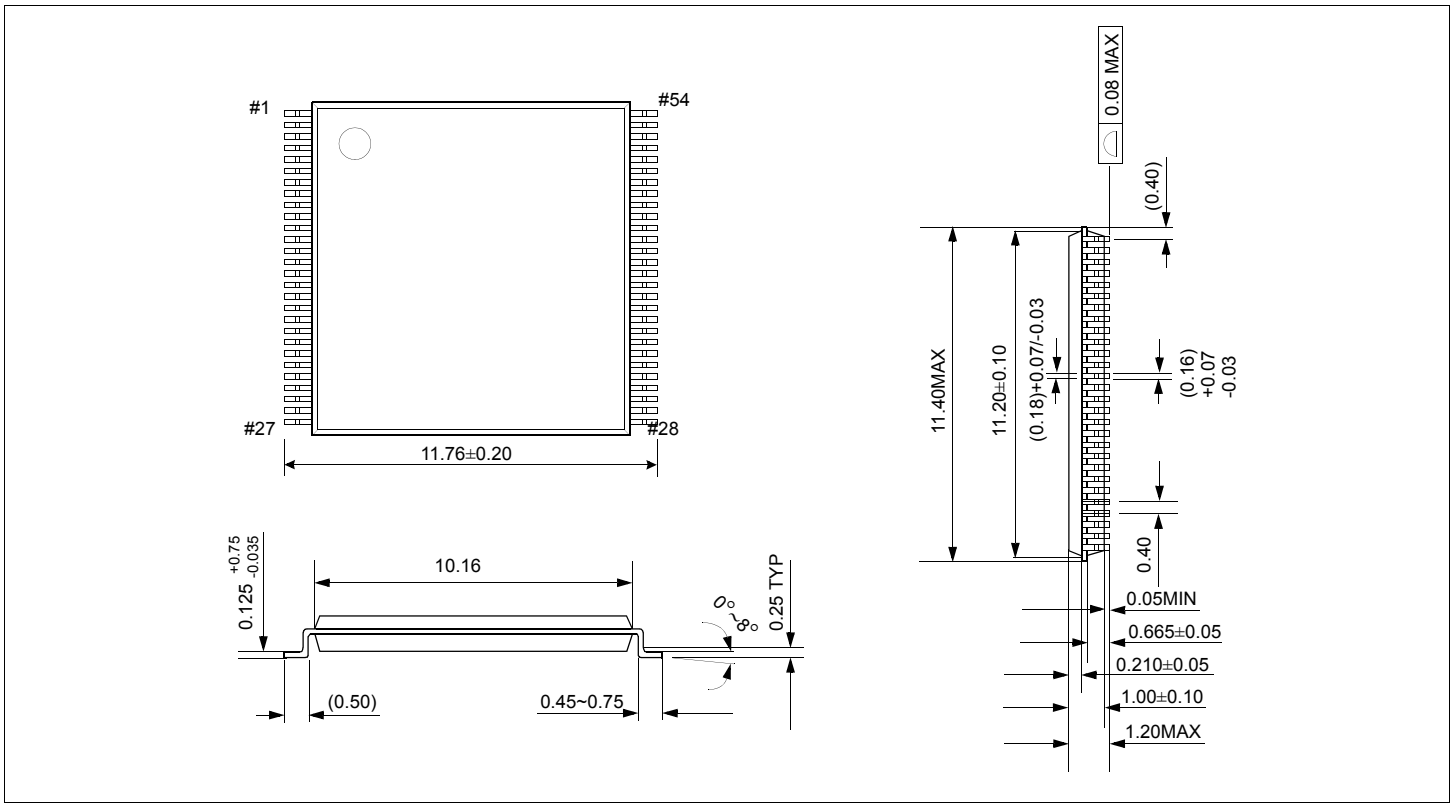


NOTE
1. ( ) IS REFERENCE
2. [ ] IS ASS'Y OUT QUALITY

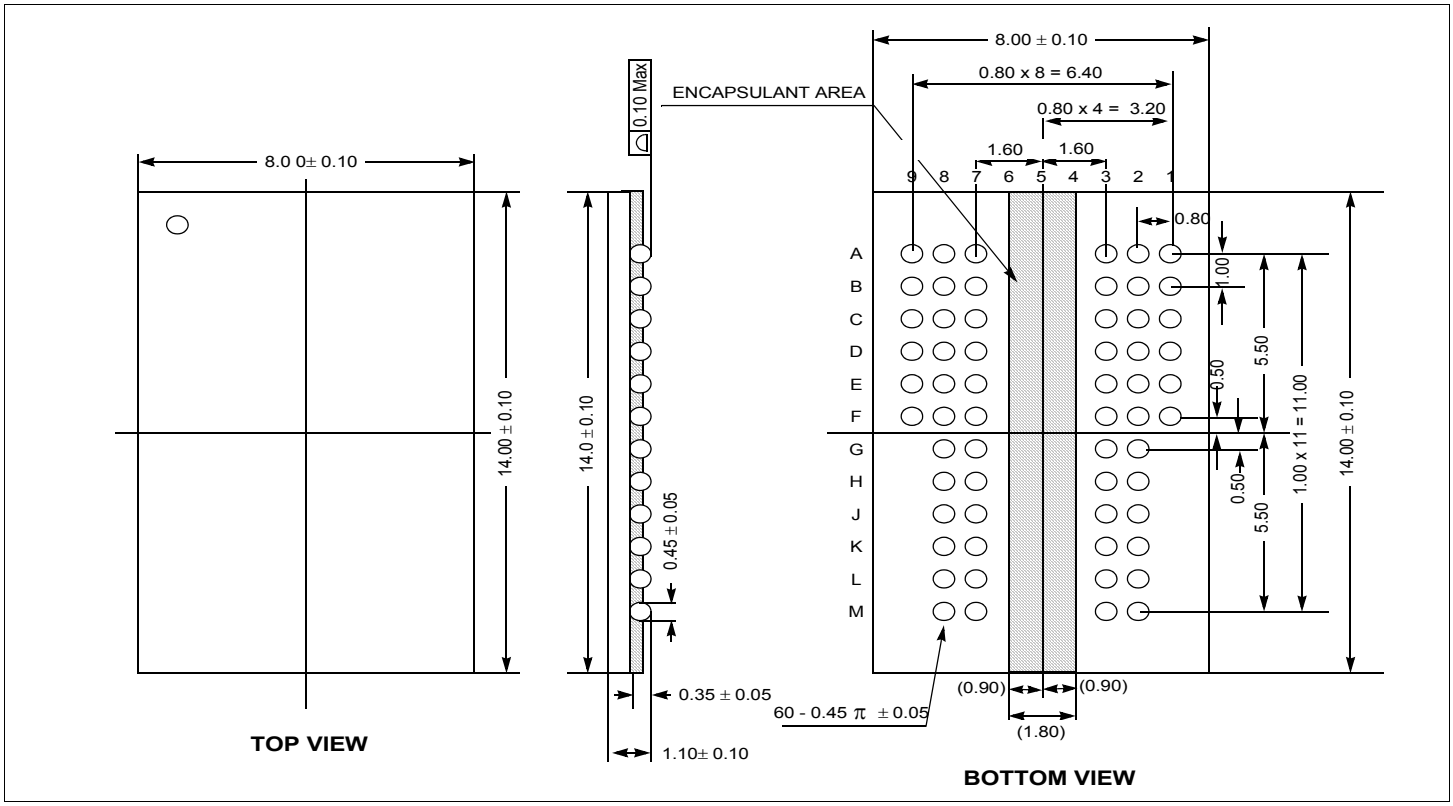
54pin sTSOP-II 300



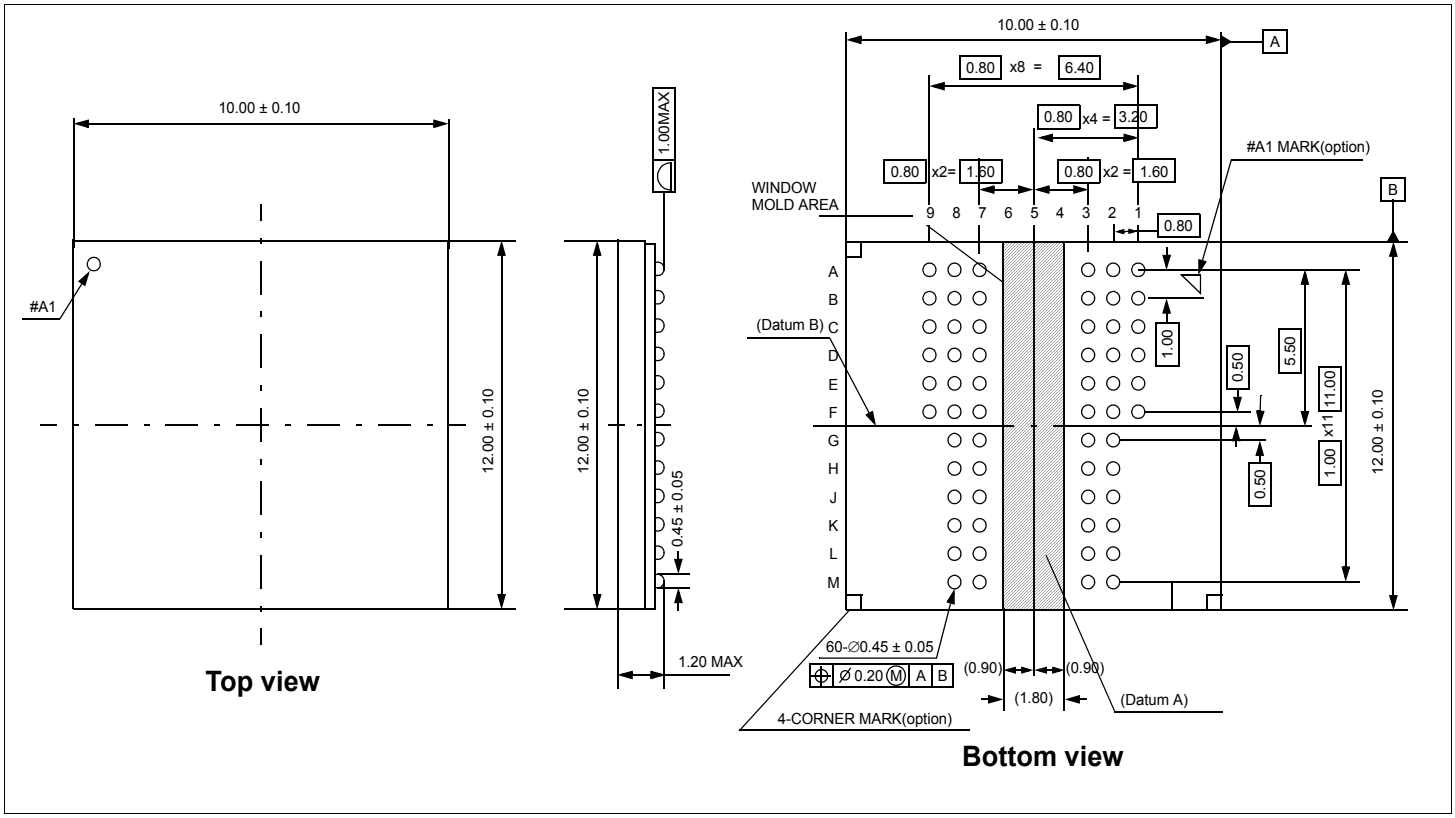
54pin sTSOP-II 400



60Ball FBGA (For 256Mb)



60Ball FBGA (For 512Mb)



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